REMARKS

This communication responds to the Final Office Action dated September 19, 2008.

Claim 1 is amended. Claims 1-26 are pending in this application. Support for the amendment to claim 1 is found generally within the patent application (*see e.g.*, FIG. 2A and page 7 lines 9-13 and lines 19-21).

§103 Rejection of the Claims

1. Claims 1-6, 8-12, 15-18 and 23-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hittman et al. (U.S. Patent No. 5,896,267, "Hittman") in view of Truex et al. (U.S. Patent No. 5,683,435, "Truex"). Applicant respectfully traverses the rejection and has amended claim 1 to clarify the present subject matter.

Applicant respectfully submits that claim 1 is allowable over the proposed combination of Hittman and Truex because the cited portions of the references do not teach or suggest all of the subject matter in the claims. For example, Applicant is unable to find in the cited portions of these references, among other things,

> a printed circuit interconnect substrate residing on the hermetic side of the hermetic seal, wherein the printed circuit interconnect substrate includes a multi-layer circuit board comprising a buried signal layer between first and second conductive layers, wherein each conductive layer is electrically connected to a constant voltage to form a constant voltage plane, and wherein the multi-layer circuit board is arranged substantially parallel to the hermetic seal and normal to the I/O conductors,

as presently recited in claim 1. As stated in the present Patent Application, this allows the filters to be placed as close as possible to the hermetic seal.[1]

The Office Action concedes that Hittman does not specifically disclose a printed circuit interconnect substrate that includes a multi-layer circuit board comprising a buried signal layer between first and second conductive layers, but states that Truex teaches a feedthrough assembly (10) ... comprising a multilayer circuit board (34) having a signal layer between first and second conductive layers.[2]

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[1] Patent Application, pg. 1 lines 26-27.
[2] Office Action, pg. 3.

However, in contrast to the present subject matter, Truex refers to a multilayered structure 34 that extends through and is hermetically sealed to the interior of the weld ring 32 at an intermediate portion 30.[3] Thus, Truex does not teach or suggest "a printed circuit interconnect substrate residing on the hermetic side of the hermetic seal," but instead resides on both sides of the hermetic seal. Additionally, the multilayered structure 34 of Truex is arranged parallel to printed conductors 56 and normal to the hermetic seal.[4] Thus, Truex with Hittman does not teach or suggest "wherein the multi-layer circuit board is arranged substantially parallel to the hermetic seal and normal to the I/O conductors," as recited in claim 1.

Further, Applicant cannot find in the cited portions of these references, "wherein one I/O conductor provides an electrical connection to the constant voltage plane" as presently recited in claim 1. Applicant cannot find in the cited portions of Hittman a connection of a lead wire 12 to a constant voltage plane, or in the cited portions of Truex, a connection of a printed conductor 56 to a constant voltage plane.

Therefore, Hittman with Truex does not teach or suggest all of the elements recited or incorporated into the claims.

Further, one of ordinary skill would not reasonably be led to combine Hittman and Truex. Hittman states that "it is critical that the filtering take place as close as to the source of the emissions as possible, such as the entrance to the housing of the implantable device."[5] In Truex the filters are placed further away from the entrance to the housing (*see*, Truex FIG. 1) than in Hittman. Thus, Hittman teaches away from Truex, and one of ordinary skill in the art would not be led to combine Hittman and Truex upon reading Hittman.

The Office states that it would have been obvious to one of ordinary skill in the art ... to have a teaching of Truex employed in the apparatus of Hittman in order to reduce noise for the apparatus. However, Hittman refers to filtered feedthrough assemblies 100, 200 that provide protection from noise. Therefore, one of ordinary skill in the art would not reasonably be led to combine Truex with Hittman to solve a problem already solved in Hittman.

Consequently, claim 1 is not obvious in view of the cited portions of Hittman and Truex. Dependent claims 2-6, 8-12, 15-18, and 23-26 are believed to be patentable for at least the

[3] Truex, col. 4 lines 38-40.
[4] Truex, FIG. 3.
[5] Hittman, col. 2 lines 50-53.

reasons set forth above. Applicant respectfully requests reconsideration and allowance of claims 1-6, 8-12, 15-18, and 23-26.

2. Claims 19-22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hittman and Truex, and further in view of Brendel et al. (U.S. Patent No. 6,529,103, "Brendel").

Applicant respectfully traverses the rejection because the cited portions of Hittman, Truex and Brendel, either separately or in combination, do not disclose, teach, or suggest some of the elements recited or incorporated into the claims. For example, Applicant cannot find

> a printed circuit interconnect substrate residing on the hermetic side of the hermetic seal, wherein the printed circuit interconnect substrate includes a multi-layer circuit board comprising a buried signal layer between first and second conductive layers, wherein each conductive layer is electrically connected to a constant voltage to form a constant voltage plane, and wherein the multi-layer circuit board is arranged substantially parallel to the hermetic seal and normal to the I/O conductors,

which is incorporated into the claims from claim 1. Consequently, Applicant respectfully requests reconsideration and allowance of claims 19-22.

3. Claims 13-14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hittman and Truex, and further in view of Andresakis et al. (U.S Patent No. 6,657,849, "Andresakis").

Applicant respectfully traverses the rejection because the cited portions of Hittman, Truex and Andresakis, either separately or in combination, or when combined with the reasoning of the Office Action, do not disclose, teach, or suggest some of the elements recited or incorporated into the claims. For example, Applicant cannot find

> a printed circuit interconnect substrate residing on the hermetic side of the hermetic seal, wherein the printed circuit interconnect substrate includes a multi-layer circuit board comprising a buried signal layer between first and second conductive layers, wherein each conductive layer is electrically connected to a constant voltage to form a constant voltage plane, and wherein the multi-layer circuit board is arranged substantially parallel to the hermetic seal and normal to the I/O conductors,

which is incorporated into the claims from claim 1. Consequently, Applicant respectfully requests reconsideration and allowance of claims 13-14.

4. Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hittman and Truex, and further in view of Chee (U.S. Patent No. 6,657,133). Applicant respectfully traverses the rejection because the cited portions of Hittman, Truex, and Chee, either separately or in combination, or when combined with the reasoning of the Office Action, do not disclose, teach, or suggest some of the elements recited or incorporated into the claims. For example, Applicant cannot find

> a printed circuit interconnect substrate residing on the hermetic side of the hermetic seal, wherein the printed circuit interconnect substrate includes a multi-layer circuit board comprising a buried signal layer between first and second conductive layers, wherein each conductive layer is electrically connected to a constant voltage to form a constant voltage plane, and wherein the multi-layer circuit board is arranged substantially parallel to the hermetic seal and normal to the I/O conductors,

which is incorporated into claim 7 from claim 1. Applicant respectfully requests reconsideration and allowance of claim 7.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's representative at (612) 371-2172 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on January 19, 2009.

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